UNITED STATES PATENT AND TRADEMARK OFFICE

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO   80527-2400

EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/898,351	SUBRAHMANYAM ET AL.
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *19 June 2006*.

2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1,2,4-12,14-17,19 and 20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1,2,4-12,14-17,19 and 20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 6/19/2006.

As indicated in Applicant's response, claims 1, 6, 9, 11, 16 have been amended. Claims

1-2, 4-12, 14-17, 19-20 are pending in the office action.

Specification

2.   The disclosure is objected to because of the following informalities: The abstract and the

disclosure contain sections or portions that recite *storing a plurality of counters* or storing a

counter, or storing a code block counter (*). Common accepted meaning for a *counter* is that it

is a software/hardware instrument to track/record value or count as such value/count is being

incremented or decremented relative to a mostly automated counting process. The instant

Specifications has made it clear that only a value from such counter – Frequency counter value --

is stored or copied (Specifications, pg. 13-15, top pg. 16); yet inconsistently enough, there are

places therein that still describe this storing/copying as 'storing a counter' or 'plurality of

counters'. Without deliberate and explicit defining in the Specifications that by reciting *counter*

the invention intends for it to actually mean a *value* or a *count*, the syntactic usage of *counter* in

the above storing/copying (*) context (i.e. the entity stored/copied being just a value or

frequency counter number – see bottom pg. 13) will be construed as idiomatic, linguistically

improper.

Appropriate and extensive correction is recommended.

Claim Objections

3.   Claims 1, 6, 11, 16 are objected to because of the following informalities: the use of

'storing each said counter of said block of code' (claims 1, 11) or 'storing said counter of a

specific block of code' (claim 16) or 'storing said counting means of said ... blocks of code'

(claim 6). From the disclosure, the block of code frequency counter value appears to be the

entity being recorded, not a *counter*, which is also a *counting means* as recited. A frequency

counter and a counter are usually construed as functional entities working on values or counts

that can be stored or incremented. One skill in the art would perceive a *counter* and *counting*

means as to be equivalent active entities operable to maintain and keep track of object elements

such as counts. The Specifications does not teach that the *block counter 25* or *storage memory*

23 are used to store a counter, but to store a frequency counter --or a VALUE thereof --

corresponding to some block of code (see Specifications: pg. 12, line 20; pg 13, lines 6-7,

bottom). The language of 'storing ... counter of ... block of code' has to be readjusted to

express storing of a count, a frequency counter value, or an entry within a counting means. Any

dependent claims reciting the same deficient terminology as the base claims would also have to

be corrected. The deficient terminology will be treated as though the recited counter is actually

the count or some frequency value, an entry tracked within a counting device or software

procedure.

4.   The reciting of 'storing each ... counter of ... code previously executed on said code

cache after said block of code is evicted from said code cache' (claims 1, 11, 16) appears

grammatically correct yet semantically confusing as to a time-related relationship between the

elements or actions being recited (e.g. after said ...code is evicted; that is, are they concurrent or

achieved in an ordered sequence?); and the language construction has to be readjusted for

enabling a much clearer interpretation.

        Appropriate correction is required.

Claim Rejections - 35 USC § 101

5.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6.   Claims 1, 6, 11, 16 along with claims 2, 5, 7, 10, 12, 15, 17 and 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, claims 1, 6, 11, 16 recite having a counter to track code cache execution of a given block; storing each of said executed code cache block in a counter cache as long as said block is in said code cache; and maintaining a distinct area, or *storage area*, to store said cached counter of any block from said code cache, after such block has been evicted from said code cache. As claimed, the system comprising some cache counting means and memory storage; or a method therefor, there appears to be missing action or some logic as to how the cached counter can be used in relation to the eviction process – when in fact there is no action of evicting being realized per se -- so to reasonably convey a real result that would affect the so-called *storage area* in order for the storage area to be of some use. Lacking teaching that would reasonably establish actual interaction between the elements interpreted as cache counter, the eviction of block of code and the final storage of counter, there appears to be no actual achievement so to effectuate the storing in order for a concrete real-world result, tangible and useful can be perceived from the claimed storage implementation as recited.

The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a " useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

As a whole, claims 1, 11, and 16 amount to entities that do not interact with each other in reasonable way as to convey that some useful entities in terms of real-world concrete, tangible result would be yielded therefrom. The claims amount to non-practical application and are rejected for leading to non-statutory subject matter.

Claims 2, 5, 7, 10, 12, 15, 17 and 20 fail to remedy to the lack of usefulness of the recited entities in order to convey a existence of a Practical Application result; hence are also rejected for non-statutory subject matter.

Claim Rejections - 35 USC § 112

7.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8.   Claims 1-2, 4-12, 14-17, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, claims 1, 6, 11, and 16 recites 'wherein said counter is not required to be added to said block of code in said code cache' (line 5, 7, 7, 4 of respective claims). The subject matter describing how this requirement is implemented does not appear to be described in the original disclosure. One skill in the art is not apprised on how such adding of counter into a code cache can be or cannot be a required limitation from any drawing or related text in the Specifications describing implementation or interaction of code cache, a new program counter, a

block counter cache and a area to store the counter of the block being evicted. The inventor

appears to fail to support how this added subject matter is construed in the invention at the time

the Application was filed; and it is deemed that the inventor is not in possession of this claimed

limitation. In light of which, this limitation would be treated without weight, i.e. meaning said

counter can be part of code cache or in any cache or memory in general.

The dependent claims 2, 4-5, 7-10, 13-15, 17, 19-20 will be rejected for not remedying to

the above lack of description deficiency.

Claim 6 recites a distinct 'storage area for storing counting means of ... blocks of code

that are most recently executed ...' (last paragraph). From the disclosed usage of *storage area*

23 (Specs: pg. 2, 3rd para; pg. 11, top para; pg. 13, bottom; pg. 16, top para), there is no evidence

that the counter value being stored therein relates to the *most recently executed* block of code.

This lack of teaching will be treated as though the storage area is to store some cached entry

corresponding to previously executed block of code in the code cache.

Claims 7-10 for failing to remedy to the above deficiency, are also rejected for dependent

to the base claims.

Claim 9 recites 'copying ... least ... executed block of code ... to said storage area when

... cache is full' (lines 7-8). This claimed subject matter (*copying ... of block of code*) is not

described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. The only depiction about storing anything in the *storage area 23* (Specs, pg. 11, top

para; pg. 13, bottom; pg. 16, top para) is about storing a frequency counter value of a block. The

claimed limitation is not described or supported in the Specifications, therefore will be treated as

though only some counter value is stored; and so only in the extent that such teaching has been

taught from the earlier claims.

9.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

10.   Claims 1, 11, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

Claim 1, 11 and 16 recites 'storing … counter of said block of code previously executed

on said code cache after said block of code is evicted from said code cache' (last paragraph of

respective claims). One skill in the art would not be able to see a clear teaching from the

language as presented. Particularly, the phrase 'code previously executed on said code cache

after said … code is evicted from said … cache' is not conveying a clear and definite time frame

as to teach where and what is considered executed and so in which time context. In terms of

code cache, one skill in the art would construe a block being stored thereon more than a block

being executed thereon. Moreover, the claim does not make it clear that the execution as recited

occurs after or before the code is evicted; or that the storing is done after the code eviction with

the execution being over, or being done only if the code after being evicted is now re-executed in

the cache – which is also one possible interpretation. There is no clear relationship between the

storing and the timeframe of execution in relation to the being evicted event. This lack of

definiteness would be treated as though the *storing* is effected after some uncorrelated eviction

event and possibly done concurrent with a code that has been previously executed.

Dependent claims 2, 4-5, 12, 14-17, 19-20 are also rejected for not clarifying on the

indefiniteness of the base claims.

Claim Rejections - 35 USC § 102

11.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

12.   Claims 1-2, 4-7, 11-12, 14-17, 19-20 are rejected under 35 U.S.C. 102(e) as being

anticipated by Burton et al., 6,738,865 (hereinafter Burton).

As per claim 1, Burton discloses a method to analyze a computer program that includes a

plurality of block of code, the method comprising:

receiving a block of code instruction in code cache (e.g. Cache 2, *entries 4a, 4b, 4c, 4d*

4e – Fig. 1);

using a counter for tracking each time said code instruction is loaded for execution (e.g.

Time counter 18 – Fig. 1) wherein said counter is not required to be added to said cache (Note:

this counter can be added or not added, i.e. no real requirement – see USC 112, 1st paragraph);

maintaining a counter cache for storing each said counter of said block code (e.g. *entries*

4a, 4b, 4c, 4d 4e – Fig. 1 – Note: entry reads on numbered array divisions having a count value

each) while said block of code is stored on said code memory, said counter cache being distinct

from code cache;

Burton optimizes the use of fast memory with LRU policy and teaches a cached counter

and an array of prioritized entries in code cache to tracking priority levels of code execution (see

LRU, cache, counter 18 – Fig. 1; see Fig. 2-3) and storing of destaged entries from said code

cache counter by means of the LRU logic approach identfying those demoted or destaged

block/entries for LRU eviction. Burton has disclosed maintaining of a storage area distinct from

the cached counter and the code cache for storing each said counter (or numerical cached entries)

said block of code previously executed such that this same block is being demoted or promoted

(see Fig. 2-3 – Note: for lack of definiteness, as pointed out from the USC 112, 2nd paragraph,

i.e. the teaching of the disclosure not read into the claims), which is equivalent to the event after

which some of the same code has been evicted (demoted from high priority) from said code

cache structure (see Cache Entries – Fig. 1) and then reasserted (and promoted again) in this

LRU list after a algorithmic analysis.

As per claim 2, see Burton for the concept of determining whether a cache is full (see

LRU, threshold - Fig. 3).

As per claim 4, Burton discloses determining which of said counter of said block of code

stored on said counter cache is least recently executed; and further teaches maintaining the least

recently executed entry of the cached block of code in a LRU list, i.e. after evicting or destaging

said least recently executed block of code related to said counter the cached entries (re claim 1

and the LRU related teachings by Burton – see Fig. 2-3; *entries 4a, 4b, 4c, 4d 4e* – Fig. 1).

As per claim 5, Burton discloses

checking said storage area to determine if said block of code is being executed for other

than the first time; loading said counter associated with said block of code being executed for

other than the first time; and updating said counter associated with said block of code being

executed for other than the first time (Note: Re claim 1 - the instituting of a *counter 18* is to

keep track with a code block that is being executed every time – including second time -- for its

count to be updated in the counter; and the fact that its counter value being computed so to be be

determined as cached *entries 4a, 4b, 4c, 4d 4e* – Fig. 1 reads on updating the counting entries in

the code cache).

    As per claim 6, Burton discloses a method to analyze a computer program that includes a

plurality of blocks of code, the method comprising means for:

    executing said computer program; counting one of said plurality of blocks is executed

(e.g. Fig. 2A-B);

    maintaining a code cache for storing one of a plurality of blocks of code derived from

said computer program (*entries 4a, 4b, 4c, 4d 4e* – Fig. 1);

    maintaining for counting each time one of said blocks of code instruction is executed

(e.g. Time counter 18 – Fig. 1) wherein said counting means is not required to be added to said

cache (Note: this counter can be added or not added, i.e. no real requirement – see USC 112, 1st

paragraph);

    maintaining a counter cache for storing each said counting means of said blocks code

most recently executed (e.g. *entries 4a, 4b, 4c, 4d 4e* – Fig. 1 – Note: entry reads on numbered

array divisions having a count value each – Note: LRU in Fig. 2-3 reads on most recently

executed), said counter cache being distinct from code cache (Note: Fig. 1 shows distinct

entities);

maintaining a counter in a storage area for storing said counting means of said blocks of code that are executed (e.g. Fig. 2-3 – Note: blocks of code that have been previously executed, as most recently or least recently being maintained in the LRU list reads on plurality of blocks that are most recently executed as per the USC 112, 2nd para analysis), with said storage area distinct from the cached counter and the code cache as shown in Figure 1.

As per claim 7, this limitation is rejected using the same rationale as set forth in claim 2.

As per claim 11, this is a computer readable medium having computer readable program code embodied therein to perform when executed a method for analyzing a computer program that includes a plurality of blocks of code comprising logic to perform the same steps as recited in claim 1; hence is rejected with the corresponding rejection as set forth therein.

As per claims 12, 14, and 15, these claims correspond to claims 2, 4, and 5, respectively; hence are rejected using the corresponding rejections as set forth therein.

As per claim 16, this claim is the system version of claim 1, hence is rejected with the corresponding rejection as set forth therein.

As per claims 17, 19, and 20, these claims correspond to claims 2, 4, and 5, respectively; hence are rejected using the corresponding rejections as set forth therein

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14.   Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton et al.,

6,738,865.

As per claim 8, in view of the techniques taught by Burton (see Fig. 2-3) and the

rationale in claim 7, the limitation of copying blocks from counter cache to a storage area when

the counter cache is full would also be obvious in light of the knowledge on why a LRU is used

and Burton's teachings (see Burton: Fig. 3; *demoted, destaged* - col. 4, lines 6-34). One skill in

the art would apply storing away the least used data to a storage when the cache threshold is

threatened as taught by well-known practices or Burton's demoting (demoted or destaged)

method so that when cache is full applying the LRU technique to maintaining the entries of

cached code considered not recently used to a stored structure (e.g. LRU structure) as mentioned

above until later analysis would provide the restoring of the evicted block entries (promoting

after destaging) back into the code cache, as this is a well-known LRU practice applying on

cache storage including the likes of Burton's approach as to have least used code be evicted or

stored away from fast memory to salvage storage resources therein as set forth in claim 1.

As per claim 9, Burton teaches cache recording of LRU(least recently used) information

(Fig. 2) in conjunction with demoting cache entries so they are stored into secondary area (re

claim 1, 2). The limitation as to determining which of the counting means of code blocks is least

recently used and copying said block of code to a storage area when the cache is full would also

have been obvious using the rationale as set forth in claim 8 above (Note: the concept of evicting

a block of code to a storage area is not supported by the Specifications, see USC 112, 1st

paragraph, hence will be treated as a mere evicting step without weight be given to where the

evicted code would be stored).

As per claim 10, this claim includes limitation of claim 5 and is rejected using the corresponding rationale as set forth in claim 5.

Response to Arguments

15.   The Applicants' arguments as submitted in the response filed 6/19/2006 are considered but are moot in light of the new grounds of rejection.

The claims are rejected as set forth in the Office Action.

Conclusion

16.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
Patent Examiner,
Art Unit 2193
September 9, 2006